CLAIMS

We Claim:

1 A biphase-mark decoding system, comprising:

a programmable clock;

a data buffer;

a receiver module coupled to the data buffer for,

receiving an external biphase-mark input stream,

recovering timing information from the input stream, and

decoding the input stream to generate decoded data and storing the decoded data in the data buffer;

an audio out module coupled to the buffer and the programmable clock for

reading the decoded data from the data buffer at a rate determined by the programmable clock; and

a processor coupled to the receiver module for executing a software-based frequency locked loop that uses the timing information from the receiver module to calculate a sampling frequency of the input stream, and then adjusts a frequency of the programmable clock to substantially match the sampling frequency so that the audio out module reads the decoded from the buffer at substantially the same rate that the receiver module inputs the decoded data into the data buffer.

2 The system of claim 1 further including a system clock coupled to the receiver module.

3 The system of claim 2 wherein the programmable clock is coupled to the receiver module and the receiver module uses either the programmable clock or the system clock to determine the timing information from the input stream.

4 The system of claim 3 wherein the system clock is capable of significantly higher frequencies than the programmable clock.

5 The system of claim 3 wherein the system clock is used to determine the timing information of the input stream at system startup, thereafter the programmable clock may be used.

6 The system of claim 1 wherein the frequency locked loop is implemented by system control software executed by the processor.

7 The system of claim 1 wherein the receiver module extracts 1T timing from the input stream using only "M" or "X" preamble patterns.

8 The system of claim 7 wherein the receiver module identifies the "M" or "X" preamble by two consecutive 3T intervals followed by two 1T intervals.

9 The system of claim 8 wherein the receiver module utilizes an adaptive jitter tolerance window for accepting clock edges in the input stream that arrive early or late.

10 The system of claim 9 wherein the jitter window is established by measuring

1T timing as a predefined number of system clock cycles, and then dividing the predefined number clock cycles by any number divisible by two as a cost-effective method to provide a jitter window that is proportionate to the input sampling frequency.

11 The system of claim 10 wherein the receiver module further includes a 1T cycle detector and jitter filter logic for establishing 1T timing of the input stream.

12 The system of claim 11 wherein the jitter window is defined by determining a lower and upper limit of the 1T interval, which is adjustable by system control software executing on the processor, and the 1T cycle detector determines a 1T timing value based on the lower and upper limit.

13 The system of claim 12 wherein the 1T cycle detector measures a time interval between edge transitions in the input stream 112 by counting a number of system clock cycles that occur between transitions of adjacent rising edges or adjacent falling edges in the input stream.

14 The system of claim 2 wherein the timing information used to calculate the sampling frequency includes a count of a number of system clock cycles or programmable clock cycles, and a count of a number of sub-frames detected in the input stream.

15 The system of claim 14 wherein the receiver module uses a clock counter register to maintain a count of number of system clock cycles or programmable

clock cycles, and uses a sub-frame counter register to maintain a count of sub-frames occurring in the input stream.

16 The system of claim 15 wherein values of the clock counter register and the sub-frame counter register are reported to the system control software when the clock counter register is full.

17 The system of claim 16 wherein the system control software calculates the sampling frequency by:

Sample Freq.= (sub-frame counter value / (2 * clock counter value)) * clock frequency.

18 The system of claim 17 wherein the receiver module compares the values of the clock counter register and the sub-frame counter register with expected values indicated by the system control software, and if the differences pass a predetermined threshold, then the receiver module generates an interrupt to notify the system control software of a change in the input stream frequency.

19 The system of claim 2 wherein the receiver module reports an occurrence of a bad input stream to the system control software using a bad signal interrupt.

20 The system of claim 19 wherein the bad signal interrupt is generated if any predefined conditions occur, including;

edge-to-edge interval of 4T or longer is detected,

a 3T edge-to-edge interval appears in a data window,

a preamble is not detected when expected, and

a preamble is detected at a wrong position.

21 A method for decoding a biphase-mark input stream, comprising:

(a) receiving an external biphase-mark input stream by a receiver module;

(b) recovering timing information from the input stream;

(c) decoding the input stream to generate decoded data and storing the decoded data in a data buffer;

(d) reading, by an audio out module, the decoded data from the data buffer at a rate determined by a programmable clock;

(e) using the timing information from the receiver module to calculate a sampling frequency of the input stream; and

(f) adjusting a frequency of the programmable clock to substantially match the sampling frequency so that the audio out module reads the decoded data from the buffer at substantially the same rate that the receiver module inputs the decoded data into the data buffer.

22 The method of claim 21 further including the step of: calculating the sampling frequency using a software-based frequency locked loop.

23 The method of claim 22 further including the step of: coupling a system clock to the receiver module.

24 The method of claim 23 further including the step of: using either the programmable clock or the system clock to determine the timing information from the input stream.

25 The method of claim 24 wherein the system clock is capable of significantly higher frequencies than the programmable clock.

26 The method of claim 25 further including the step of: using the system clock to determine the timing information of the input stream at method startup, and thereafter optionally using a programmable clock.

27 The method of claim 21 wherein the receiver module extracts 1T timing from the input stream using only "M" or "X" preamble patterns.

28 The method of claim 27 wherein the receiver module identifies the "M" or "X" preamble by two consecutive 3T intervals followed by two 1T intervals.

29 The method of claim 28 further including the step of: using an adaptive jitter tolerance window for accepting clock edges in the input stream that arrive early or late.

30 The method of claim 29 further including the step of: establishing the jitter window by measuring 1T timing as a predefined number of system clock cycles, and then dividing the predefined number of clock cycles by any number divisible by two to provide a jitter window that is proportional to the input sampling frequency.

31 The method of claim 21 wherein the timing information used to calculate the sampling frequency includes a count of a number of system clock cycles or programmable clock cycles, and a count of a number of sub-frames detected in the input stream.

32 The method of claim 31 wherein the method control software calculates the sampling frequency by:

Sample Freq.= (sub-frame counter value / (2 * clock counter value)) * clock frequency.

33 The method of claim 32 wherein the receiver module compares the values of the clock counter register and the sub-frame counter register with expected values indicated by the method control software, and if the differences pass a predetermined threshold, then the receiver module generates an interrupt to notify the method control software of a change in the input stream frequency.

34 The method of claim 21 wherein the receiver module reports an occurrence of a bad input stream to the method control software using a bad signal interrupt.

35 The method of claim 34 further including the step of: generating the bad signal interrupt if any predefined conditions occur, including;

edge-to-edge interval of 4T or longer is detected,

a 3T edge-to-edge interval appears in a data window,

a preamble is not detected when expected, and

a preamble is detected at a wrong position.

36 A biphase-mark decoding system, comprising:

a system clock;

a audio clock;

a data buffer;

a receiver module coupled to the system clock, the audio clock, and the data buffer, the receiver module for receiving an external biphase-mark input stream,

recovering timing information from the input stream using either the system clock or the audio clock, and

decoding the input stream to generate decoded data and storing decoded data in the data buffer;

an audio out module coupled to the data buffer and the audio clock for reading the decoded data from the data buffer at a rate determined by the audio clock and for generating output data; and

a processor coupled to the receiver module and the audio clock for executing control software that implements a frequency locked loop, whereby the control software receives the timing information from the receiver module and uses the timing information as an error measurement to continually adjust a frequency of the audio clock to cause the audio out module to read the decoded data from the data buffer at substantially the same rate that the decoder inputs the decoded data to the data buffer.

37 The system of claim 36 wherein the control software calculates a sampling frequency from the timing information and adjusts the frequency of the audio clock to substantially match the sampling frequency.

38 The system of claim 36 wherein the timing information includes a count of a number of system clock cycles and a count of a number of sub-frames detected in the input stream.

39 The system of claim 36 wherein the timing information includes a count of a number of programmable audio clock cycles and a count of a number of sub-frames detected in the input stream.